AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (previously presented) A method comprising:

receiving a first digital control value establishing a phase of a first clock signal;

receiving a second digital control value establishing a phase of a second clock signal; and

comparing the first and second digital control values to detect a phase relationship between the first and second clock signals.

2. (previously presented) The method of claim 1, wherein the phase relationship between the first and second clock signals varies with PVT (process, voltage, and temperature) variations, the method further comprising adjusting a PVT-sensitive circuit as a function of the detected phase relationship between the first and second clock signals.

3. (previously presented) The method of claim 1, further comprising:

calibrating the phase of the first clock signal relative to a received data signal;

clocking an input latch with the first clock signal to latch the received data signal and to provide a captured data signal; and

latching the captured data signal at a time that varies as a function of the detected phase relationship between the first and second clock signals to provide a synchronized data signal.

4. (previously presented) The method of claim 1, further comprising:

calibrating the phase of the second clock signal relative to a received third clock signal;

identifying the phase of the third clock signal relative to the first clock signal with reference to the detected phase relationship between the first and second clock signals.

5. (previously presented) A method comprising:

receiving a first digital control value establishing a phase of a first clock signal;

receiving a second digital control value establishing a phase of a second clock signal;

comparing the first and second clock signals in a calibration procedure while varying the second digital control value to provide a predetermined phase relationship between the first and second clock signals;

deriving a correction value from the second digital control value that provides the predetermined phase relationship between the first and second clock signals; and

subsequent to the calibration procedure, compensating the second digital control value with the correction value to account for different propagation delays of the first and second clock signals.

6. (previously presented) A device comprising:

a first clock generator to generate a first clock signal in response to a first digital control value, wherein the first digital control value establishes a phase of the first clock signal;

a second clock generator to generate a second clock signal in response to a second digital control value, wherein the second digital control value establishes a phase of the second clock signal; and

a phase detection logic to compare the first and second digital control values to detect a phase relationship between the first and second clock signals.

7. (previously presented) The device of claim 6, further comprising a PVT (process, voltage, and temperature) sensitive circuit that is responsive to the phase detection logic to compensate for PVT variations.

8. (previously presented) The device of claim 6, further comprising:

a calibration logic to set the first digital control value to calibrate the phase of the first clock signal relative to a received data signal;

an input latch clocked by the first clock signal to latch the received data signal and to provide a captured data signal; and

a latching logic, in response to the phase relationship, to latch the captured data signal to provide a synchronized data signal relative to the second clock signal.

9. (previously presented) The device of claim 6, further comprising:

a calibration logic to receive a third clock signal having an undetermined phase relative to the first clock signal and to set the second digital control value to calibrate the phase of the second clock signal relative to the third clock signal;

wherein the phase detection logic compares the first and second digital control values to determine a phase of the third clock signal relative to the first clock signal.

10. (previously presented) A device comprising:

a first clock generator to generate a first clock signal in response to a first digital control value, wherein the first digital control value establishes a phase of the first clock signal;

a second clock generator to generate a second clock signal in response to a second digital control value, wherein the second digital control value establishes a phase of the second clock signal;

a calibration logic that operates in a calibration procedure to compare the first and second clock signals while varying at least one of the first and second digital control values to provide a predetermined phase relationship between the first and second clock signals;

wherein the calibration logic derives at least one correction value from at least one of the first and second digital control values that provide the predetermined phase relationship; and

wherein the calibration logic compensates at least one of the first and second digital control values with the at least one correction value to account for different propagation delays of the first and second clock signals.

11. (previously presented) A method of phase detection, comprising:

receiving a clock signal that has an undetermined phase relative to a reference clock signal;

generating a measurement clock signal having a phase that is established relative to the reference clock signal by a phase control value;

setting the phase control value to provide a predetermined phase relationship between the measurement clock signal and the received clock signal; and

evaluating the phase control value to detect a measured phase relationship of the received clock signal relative to the reference clock signal.

12. (previously presented) The method of claim 11, wherein setting the phase control value comprises varying the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the received clock signal.

13. (previously presented) A phase detection device, comprising:

a clock generator to generate a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

a calibration logic to vary the phase control value to provide a predetermined phase relationship between the measurement clock signal and a received clock signal that has an undetermined phase; and

an evaluation logic to evaluate the phase control value to detect a phase relationship between the received clock signal and the reference clock signal.

14. (previously presented) The phase detection device of claim 13, wherein the calibration logic varies the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

15. (previously presented) A method comprising:

generating a plurality of clock signals in response to a plurality of digital control values that specify a plurality of relative phases of the clock signals, the clock signals having different propagation delays;

varying the digital control values in a calibration procedure to provide a plurality of predetermined phase relationships between the clock signals;

deriving a plurality of correction values from the digital control values that provide the predetermined phase relationships;

subsequent to the calibration procedure, setting the digital control values to provide the relative phases of the clock signals; and

compensating the digital control values with the correction values to account for the different propagation delays of the clock signals.

16. (previously presented) The method of claim 15, wherein the plurality of clock signals have approximately identical phases when in the predetermined phase relationships.

17. (previously presented) The method of claim 15, wherein generating the plurality of clock signals comprises deriving the plurality of clock signals from one or more common reference clock signals.

18. (previously presented) A device comprising:

a plurality of clock generators to generate a plurality of clock signals in response to a plurality of digital control values that specify a plurality of relative phases of the clock signals, the clock signals having different propagation delays;

a calibration logic to vary the digital control values in a calibration procedure to provide a plurality of predetermined phase relationships between the clock signals; and

wherein the calibration logic derives one or more correction values from the digital control values to provide the plurality of predetermined phase relationships, the one or more correction values being used subsequent to the calibration procedure to account for the different propagation delays of the clock signals.

19. (previously presented) The device of claim 18, wherein the plurality of clock signals have approximately identical phases when in the predetermined phase relationships.

20. (previously presented) The device of claim 18, wherein the plurality of clock generators generate the plurality of clock signals from one or more common reference clock signals.

21. (previously presented) A method of phase detection, comprising:

generating a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

delaying the measurement clock signal by a delay that varies with PVT (process, voltage, and temperature) variations to obtain a delayed measurement clock signal;

varying the phase control value to obtain a digital PVT adjustment value that provides a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal; and

adjusting a PVT-sensitive circuit as a function of the digital PVT adjustment value to compensate for the PVT variations in the PVT-sensitive circuit.

22. (previously presented) The method of claim 21, wherein varying the phase control value comprises varying the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

23. (previously presented) A device comprising:

a clock generator to generate a measurement clock signal having a phase that is established relative to a reference clock signal by a phase control value;

one or more delay elements to delay the measurement clock signal by a delay that varies with PVT (process, voltage, and temperature) variations to obtain a delayed measurement clock signal;

a calibration logic to vary the phase control value to obtain a digital PVT adjustment value that provides a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal; and

a PVT-sensitive circuit, responsive to the digital PVT adjustment value, to compensate for the PVT variations in the PVT-sensitive circuit.

24. (previously presented) The device of claim 23, wherein the calibration logic varies the phase control value until the phase of the measurement clock signal is approximately equal to the phase of the reference clock signal.

25. (previously presented) A method of synchronizing a received data signal with a target timing signal, comprising:

generating an input timing signal having a phase that is established relative to the target timing signal by an input phase control value;

setting the input phase control value to calibrate the phase of the input timing signal relative to the received data signal;

clocking the received data signal with the input timing signal to provide a captured data signal;

evaluating the input phase control value to determine a timing phase to clock the captured data signal for synchronization with the target timing signal; and

clocking the captured data signal at the timing phase to provide a synchronized data signal relative to the target timing signal.

26. (previously presented) The method of claim 25, wherein the evaluating comprises comparing the input phase control value to a reference value.

27. (previously presented) The method of claim 25, wherein:

the evaluating comprises comparing the input phase control value to a reference value; and

the reference value represents a 90° phase offset from the target timing signal.

28. (previously presented) The method of claim 25, wherein the evaluating comprises comparing the input phase control value to a target phase control value that establishes the phase of the target timing signal.

29. (previously presented) The method of claim 25, further comprising:

generating the target timing signal in response to a target phase control value that establishes a phase of the target timing signal.

30. (previously presented) The method of claim 25, further comprising:

generating the target timing signal in response to a target phase control value that establishes a phase of the target timing signal; and

wherein the evaluating comprises comparing the input phase control value to the target phase control value.

31. (previously presented) The method of claim 25, wherein the input phase control value is a digital value.

32. (previously presented) The method of claim 25, wherein the evaluating determines the timing phase to be (a) a phase of the target timing signal when the evaluation indicates that the target timing signal lags the input timing signal by more than 90° or (b) a phase that is 180° relative to the phase of the target timing signal when the evaluation indicates that the target timing signal lags the input timing signal by less than 90°.

33. (previously presented) The method of claim 25, further comprising:

clocking the synchronized data signal with the target timing signal.

34. (previously presented) A method of synchronizing a received data signal with a target clock signal, comprising:

setting a target phase control value to establish a phase of the target clock signal;

setting an input phase control value to establish a phase of an input clock signal;

clocking the received data signal with the input clock signal to provide a captured data signal;

comparing the target phase control value and the input phase control value to determine a timing phase to clock the captured data signal for synchronization with the target clock signal; and

clocking the captured data signal at the timing phase to provide a synchronized data signal relative to the target clock signal.

35. (previously presented) The method of claim 34, wherein the comparing comprises detecting whether the target clock signal lags the input clock signal by a predetermined amount based on the target and input phase control values.

36. (previously presented) The method of claim 34, wherein the comparing comprises detecting whether the target clock signal lags the input clock signal by 90° based on the target and input phase control values.

37. (previously presented) The method of claim 34, wherein the target and input phase control values are digital values.

38. (previously presented) The method of claim 34, wherein the comparing determines the timing phase to be (a) the phase of the target clock signal when the comparing indicates that the target clock signal lags the input timing signal by more than 90° or (b) a phase that is 180° relative to the phase of the target clock signal when the comparing indicates that the target clock signal lags the input clock signal by less than 90°.

39. (previously presented) The method of claim 34, further comprising:

clocking the synchronized data signal with the target timing signal.

40. (previously presented) The method of claim 34, further comprising:

setting the input phase control value to calibrate the phase of the input clock signal relative to the received data signal.

41. (previously presented) A device for synchronizing a received data signal with a target clock signal, comprising:

an input clock generator to generate an input clock signal at a calibrated phase relative to the received data signal, the input clock generator to receive an input phase control value to establish the calibrated phase of the input clock signal;

an input latch that is clocked by the input clock signal to latch the received data signal and to provide a captured data signal;

an evaluation logic to evaluate the input phase control value to determine a timing phase to clock the captured data signal for synchronization with the target clock signal; and

a latching logic to latch the captured data signal at the timing phase to provide a synchronized data signal relative to the target clock signal.

42. (previously presented) The device of claim 41, further comprising:

a target clock generator to generate the target clock signal, wherein the target clock generator receives a target phase control value to establish a phase of the target clock signal;

wherein the evaluation logic compares the target phase control value and the input phase control value to determine the timing phase.

43. (previously presented) The device of claim 41, wherein the evaluation logic compares the input phase control value to a reference value.

44. (previously presented) The device of claim 41, wherein:

the evaluation logic compares the input phase control value to a reference value; and

the reference value represents a 90° phase difference from the target clock signal.

45. (previously presented) A device as recited in claim 41, wherein the input phase control value is a digital value.

46. (previously presented) The device of claim 41, wherein the evaluation logic determines the timing phase to be (a) a phase of the target clock signal when the target clock signal lags the input clock signal by more than 90° or (b) a phase that is 180° relative to the phase of the target clock signal when the target clock signal lags the input clock signal by less than 90°.

47. (previously presented) The device of claim 41, further comprising:

a second input latch to clock the synchronized data signal in response to the target clock signal.